Remarks

Entry of the foregoing amendments and reconsideration of this application is requested. By this amendment, claims 1 and 18 has been amended to more specifically set forth the invention. Claim 4 has been amended to correct dependency. Claim 7 has been cancelled. New claims 24 and 25 have been presented herein. Claims 1-6, and 8-25 remain in the application.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1-3, 5, 7-8, and 18 under 35 U.S.C. 102(b) as being anticipated by Lothian, U.S. Patent No. 5,981,319, hereinafter referred to as Lothian. The Examiner in making this rejection states that Lothian discloses a process for forming a transistor on the surface of a wafer by forming a metallic T gate between source/drain regions on the surface of the wafer utilizing the method as claimed by the applicants.

The applicant in response has amended claims 1, 18 to more specifically state the invention as including the step of forming a resist stack including an isotropically developing material formed on an uppermost surface of the stabilized resist layer and an imageable material formed on a surface of the isotropically developing material. It is believed that this step overcomes the rejection, in that Lothian fails to disclose the forming of a multilayer resist stack in which included is an imageable material and an isotropically developing material. Lothian discloses a

base resist layer that is stabilized using a plasma treatment, thus rendering a hardened base resist layer. A second resist layer is formed on the uppermost surface of the base resist layer. The second resist layer is formed as a single layer, and thus does not include a isotropically developing interim resist layer as disclosed and claimed by the applicants.

The applicants assert that the inclusion of a multilayer resist stack enables the applicants to form a more resolute, and robust end product, in which critical dimensions are better able to be controlled. Accordingly, the applicants believe that independent claims 1 and 18 are now in a condition for allowance in light of the amendments and remarks made herein. The applicants additionally believe that claims 2, 3, 5, and 7-9 are in a condition for allowance in that they ultimately depend from claim 1. Notice to that effect is requested.

Next, the Examiner has rejected claims 1-3, 5, 7-9, and 18 under 35 U.S.C. 102(e) as being anticipated by Furukawa et al., U.S. Patent No. 6,387,783, hereinafter referred to as Furukawa. The Examiner in making this rejection states that Furukawa discloses a process for forming a transistor on the surface of a wafer by forming a metallic T gate between source/drain regions on the surface of the wafer. The Examiner asserts that the T gate is formed on the surface of the wafer using the same process steps as claimed by the applicants.

The applicant in response has amended claims 1, 18 to more specifically state the invention as including the step of forming a resist stack including an

isotropically developing material formed on an uppermost surface of the stabilized resist layer and an imageable material formed on a surface of the isotropically developing material. It is believed that this step overcomes the rejection, in that Furukawa fails to disclose the forming of a multilayer resist stack in which included is an imageable material and an isotropically developing material. Furukawa discloses a base resist layer that is stabilized using a heat or UV light, thus rendering a hardened base resist layer. A second resist layer is formed on the uppermost surface of the base resist layer. The second resist layer is formed as a single layer, and thus does not include a isotropically developing interim resist layer as disclosed and claimed by the applicants. Furukawa utilizes an image reversal process in which a retrograde profile is formed in the second resist layer. The applicants assert that this type of process is typically limited to i-line resist techniques, and thus renders a larger critical dimension.

The applicants assert that the inclusion of a multilayer resist stack enables the applicants to form a more resolute, and robust end product, in which critical dimensions are better able to be controlled. Accordingly, the applicants believe that independent claims 1 and 18 are now in a condition for allowance in light of the amendments and remarks made herein. The applicants additionally believe that claims 2, 3, 5, and 7-9 are in a condition for allowance in that they ultimately depend from claim 1. Notice to that effect is requested.

Finally, the Examiner has rejected claims 1-3, 5, 7-9, and 18 under 35 U.S.C. 102(b) as being anticipated by Kang, et al., JP 07-201,889, hereinafter referred to

as Kang. The Examiner in making this rejection states that Kang discloses a process for forming a transistor on the surface of a wafer by forming a metallic T gate between source/drain regions on the surface of the wafer. The Examiner asserts that the T gate is formed on the surface of the wafer using the same process steps as claimed by the applicants.

The applicant in response has amended claims 1, 18 to more specifically state the invention as including the step of forming a resist stack including an isotropically developing material formed on an uppermost surface of the stabilized resist layer and an imageable material formed on a surface of the isotropically developing material. It is believed that this step overcomes the rejection, in that Kang fails to disclose the forming of a multilayer resist stack in which included is an imageable material and an isotropically developing material. Kang discloses a base resist layer that is stabilized, thus rendering a hardened base resist layer. A second resist layer is formed on the uppermost surface of the base resist layer. The second resist layer is formed as a single layer, and thus does not include a isotropically developing interim resist layer as disclosed and claimed by the applicants.

The applicants assert that the inclusion of a multilayer resist stack enables the applicants to form a more resolute, and robust end product, in which critical dimensions are better able to be controlled. Accordingly, the applicants believe that independent claims 1 and 18 are now in a condition for allowance in light of the amendments and remarks made herein. The applicants additionally believe that

claims 2, 3, 5, and 7-9 are in a condition for allowance in that they ultimately depend from claim 1. Notice to that effect is requested.

35 U.S.C. 103 Rejection

The applicants assert that the subject matter of the various claims was commonly owned at the time the inventions covered therein were made.

The Examiner has rejected claims 4, 9-13, 15-17, 19-20, and 22 under 35 U.S.C. 103(a) as being unpatentable over Lothian as previously applied. The Examiner notes that Lothian fails to specifically disclose the specific usage of the types of resist materials which are claimed by the applicant and the specific means which are claimed by the applicant for removing the photo resist layers using a two step process. Accordingly, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form any of the photo resist layers in the process taught above out of any of the specific types of materials which are claimed by the applicant and to use a two step process which is claimed by the applicant for removing the photo resist layers from the wafer in the process as taught.

The applicant in response has amended claims 1, 18 to more specifically state the invention as including the step of forming a resist stack including an isotropically developing material formed on an uppermost surface of the stabilized resist layer and an imageable material formed on a surface of the isotropically

developing material. It is believed that this step overcomes the rejection, in that Lothian fails to disclose the forming of a multilayer resist stack in which included is an imageable material and an isotropically developing material. Lothian discloses a base resist layer that is stabilized using a plasma technique, thus rendering a hardened base resist layer. A second resist layer is formed on the uppermost surface of the base resist layer. The second resist layer is formed as a single layer, and thus does not include a isotropically developing interim resist layer as disclosed and claimed by the applicants. Furthermore, Lothian fails to disclose a reentrant resist profile as disclosed by the applicant. The specific configuration of the reentrant profile provides for the subsequent deposition of a metal layer without deposition in a consistent layer. The overhang reentrant profile provides for deposition of the metal layer so as to allow for the subsequent removal of the excess material leaving a resultant T-shaped gate. Lothian fail to provide for a similar reentrant profile and as a result, deposition of the metal layer forms a continuous layer across the second resist layer and the stabilized resist layer. This continuous layer precludes fabrication of a T-gate or tiered structure without additional steps to remove excess deposited metal.

The applicants assert that the inclusion of a multilayer resist stack enables the applicants to form a more resolute, and robust end product, in which critical dimensions are better able to be controlled. Accordingly, the applicants believe that independent claims 1 and 18 are now in a condition for allowance in light of the amendments and remarks made herein. The applicants additionally believe that claims 4, 9-13, 15-17, 19-20 and 22 are in a condition for allowance in that they

ultimately depend from claims 1 and 18, respectively. Notice to that effect is requested.

The Examiner has next rejected claims 4, 6, 10-17 and 19-22 under 35 U.S.C. 103(a) as being unpatentable over Furukawa as previously applied. The Examiner notes that Furukawa fails to specifically disclose the specific usage of the types of resist materials which are claimed by the applicant and the specific means which are claimed by the applicant for removing the photo resist layers using a two step process. Accordingly, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form any of the photo resist layers in the process taught above out of any of the specific types of materials which are claimed by the applicant and to use a two step process which is claimed by the applicant for removing the photo resist layers from the wafer in the process as taught.

The applicant in response has amended claims 1, 18 to more specifically state the invention as including the step of forming a resist stack including an isotropically developing material formed on an uppermost surface of the stabilized resist layer and an imageable material formed on a surface of the isotropically developing material. It is believed that this step overcomes the rejection, in that Furukawa fails to disclose the forming of a multilayer resist stack in which included is an imageable material and an isotropically developing material. Furukawa discloses a base resist layer that is stabilized using a heat or UV light, thus rendering a hardened base resist layer. A second resist layer is formed on the

uppermost surface of the base resist layer. The second resist layer is formed as a single layer, and thus does not include a isotropically developing interim resist layer as disclosed and claimed by the applicants. The applicants assert that Furukawa does not make obvious the applicants' method in that Furukawa utilizes i-line technology which generally does not provide for controlled critical dimensions. There is no disclosure in Furukawa to teach the use of a dual resist stack to achieve the critical dimension in the reentrant profile as taught by the applicant.

The applicants assert that the inclusion of a multilayer resist stack enables the applicants to form a more resolute, and robust end product, in which critical dimensions are better able to be controlled. Accordingly, the applicants believe that independent claims 1 and 18 are now in a condition for allowance in light of the amendments and remarks made herein. The applicants additionally believe that claims 4, 6, 10-17, and 19-22 are in a condition for allowance in that they ultimately depend from claims 1 and 18, respectively. Notice to that effect is requested.

Finally, the Examiner has rejected claims 4, 10-13, 15-17, 19-20 and 22 under 35 U.S.C. 103(a) as being unpatentable over Kang as previously applied. The Examiner notes that Lothian fails to specifically disclose the specific usage of the types of resist materials which are claimed by the applicant. Accordingly, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form any of the photo resist layers in the process taught above out of any of the specific types of materials which are claimed by the applicant.

The applicant in response has amended claims 1, 18 to more specifically state the invention as including the step of forming a resist stack including an isotropically developing material formed on an uppermost surface of the stabilized resist layer and an imageable material formed on a surface of the isotropically developing material. It is believed that this step overcomes the rejection, in that Kang fails to disclose the forming of a multilayer resist stack in which included is an imageable material and an isotropically developing material. Kang discloses a base resist layer that is stabilized, thus rendering a hardened base resist layer. A second resist layer is formed on the uppermost surface of the base resist layer. The second resist layer is formed as a single layer, and thus does not include a isotropically developing interim resist layer as disclosed and claimed by the applicants. The applicants assert that there is no disclosure in Kang to teach the use of a dual resist stack to achieve the critical dimension in the reentrant profile as taught by the applicant.

The applicants assert that the inclusion of a multilayer resist stack enables the applicants to form a more resolute, and robust end product, in which critical dimensions are better able to be controlled. Accordingly, the applicants believe that independent claims 1 and 18 are now in a condition for allowance in light of the amendments and remarks made herein. The applicants additionally believe that claims 4, 10-13, 15-17, 19-20. and 22 are in a condition for allowance in that they ultimately depend from claims 1 and 18, respectively. Notice to that effect is requested.

The applicants have further amended claim 4 to correct dependency on claim 1. The applicants wish to cancel claim 7, and have done so herein, in light of the amendments to claim 1.

The applicants have added new claims 24 and 25. New claims 24 and 25 disclose a multilayer resist stack in which claimed is the step of depositing a resist stack on an uppermost surface of the stabilized resist layer including the step of patterning a reentrant resist profile in the resist stack by diffusing a base into an uppermost portion of the resist stack, wherein the reentrant profile has a dimension greater than the opening defined in the stabilized resist layer. Further claimed is the step of defining an isotropically developed material adjacent the stabilized resist layer. The applicants assert that Lothian, Furukawa and Kang fail to disclose the fabrication of a multilayer resist stack in which the reentrant resist profile is formed by diffusing a base into an uppermost portion of the resist stack. Accordingly, the applicants believe claims 24 and 25 are in a condition for allowance. Notice to that effect is requested.

No amendment made herein was related to the statutory requirements of patentability unless expressly states; rather any amendment not so identified may be considered as directed *inter alia* to clarification of the structure and/or function of the invention and Applicants' best mode for practicing the same. Additionally, no amendment made herein was presented for the purpose of narrowing the scope of any claim, unless Applicant has argued that such amendment was made to

distinguish over a particular reference or combination of references. Furthermore, no election to pursue a particular line of argument was made herein at the expense of precluding or otherwise impeding Applicants from raising alternative lines of argument later during prosecution. Applicants' failure to affirmatively raise specific arguments is not intended to be construed as an admission to any particular point raised by the Examiner.

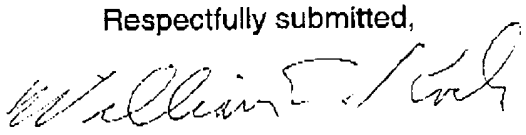
The Applicant believes that the subject application, is in condition for allowance. Such action is earnestly solicited by the Applicant. In the event that the Examiner deems the present application non-allowable, it is requested that the Examiner telephone the Applicant's attorney or agent at the number indicated below so that the prosecution of the present case may be advanced by the clarification of any continuing rejection.

CR 01-031
PATENT

SUMMARY: Reconsideration is respectfully requested. In view of the foregoing amendments and remarks it is believed that the application, including claims 1-6 and 8-25, is now in condition for allowance. Notice to that effect is respectfully requested.

Authorization is hereby given to charge any fees necessitated by actions taken herein, including any extension of time fees, to Deposit Account 502117.

Respectfully submitted,



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